UNITED STATES PATENT APPLICATION FOR:

PLANARIZED COPPER CLEANING FOR REDUCED DEFECTS

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BACKGROUND OF THE INVENTION

Related Applications

This application is a continuation-in-part of co-pending United States Patent Application No. 09/450,479 [AMAT/3976], which was filed on November 29, 1999, and is incorporated by reference herein.

Field of the Invention

The present invention relates to copper (Cu) and/or copper alloy metallization in semiconductor devices with improved planarity and reduced defects. The present invention is applicable to manufacturing high speed integrated circuits having submicron design features and high conductivity interconnect structures with improved reliability.

Background of the Related Art

The escalating requirements for high density and performance associated with ultra large scale integration semiconductor wiring require responsive changes in interconnect technology. Such escalating requirements have been found difficult to satisfy in terms of providing a low RC (resistance and capacitance) interconnect pattern, particularly in applications where submicron vias, contacts and trenches have high aspect ratios imposed by miniaturization.

Conventional semiconductor devices comprise a semiconductor substrate, typically doped monocrystalline silicon, and a plurality of sequentially formed dielectric interlayers and conductive patterns. An integrated circuit is formed containing a plurality of conductive patterns comprising conductive lines separated by interwiring spacings, and a plurality of interconnect lines. Typically, the conductive patterns on different layers, *i.e,*. are electrically connected by a conductive plug filling a via hole, while a conductive plug filling a contact hole establishes electrical contact with an active region on a semiconductor substrate, such as a source/drain region. Conductive lines are formed in trenches which typically extend substantially horizontal with respect to the semiconductor substrate. Semiconductor "chips" comprising five or more levels of metallization are becoming more prevalent as device geometries shrink to submicron levels.

A conductive plug filling a via hole is typically formed by depositing an dielectric layer on a conductive layer comprising at least one conductive pattern, forming an opening through the dielectric layer by conventional photolithographic and etching techniques, and filling the opening with a conductive material, such as tungsten (W). Excess conductive material on the surface of the dielectric interlayer is typically removed by chemical mechanical polishing (CMP). One such method is known as damascene and basically involves forming an opening in the dielectric interlayer and filling the opening with a metal. Dual damascene techniques involve forming an opening comprising a lower contact or via hole section in communication with an upper trench section. The entire opening is filled with a conductive material, typically a metal, to simultaneously form a conductive plug in electrical contact with a conductive line.

Copper (Cu) and copper alloys have received considerable attention as candidates for replacing aluminum (Al) in interconnect metallization. Copper and copper alloys are relatively inexpensive, easy to process, and have a lower resistivity than aluminum. In addition, copper and copper alloys have improved electrical properties, *vis-à-vis* tungsten (W), making copper and copper alloys desirable metals for use as a conductive plug as well as conductive wiring.

An approach to forming copper and copper alloy plugs and wiring comprises the use of damascene structures. However, due to copper diffusion through dielectric layer materials, such as silicon dioxide, a diffusion barrier layer for copper interconnect structures is provided between copper or copper alloy interconnect structures and surrounding dielectric materials. Typical diffusion barrier metals include tantalum (Ta), tantalum nitride (TaN), titanium nitride (TiN), titanium-tungsten (TiW), tungsten (W), tungsten nitride (WN), titanium-titanium nitride (Ti-TiN), titanium silicon nitride (TiSiN), tungsten silicon nitride (WSiN), tantalum silicon nitride (TaSiN) and silicon nitride for copper and copper alloys. The use of such barrier materials to encapsulate copper is not limited to the interface between copper and the dielectric interlayer, but includes interfaces with other metals as well.

In conventional CMP techniques, a wafer carrier assembly is rotated in contact with a polishing pad in a CMP apparatus. The polishing pad is mounted on a rotating turntable or platen, or moving above a stationary polishing table, driven by an external

driving force. The wafers are typically mounted on a carrier which provides a controllable pressure urging the wafers against the polishing pad. Thus, the CMP apparatus effects polishing or rubbing movement between the surface of each thin semiconductor wafer and the polishing pad while dispersing a polishing chemical with or without abrasive particles in a reactive solution to effect both chemical activity and mechanical activity while applying a force between the wafer and a polishing pad.

It is extremely difficult to planarize a copper or copper alloy surface, as by CMP of a damascene inlay, without generating a high degree of surface defects, such as corrosion, scratches, pitting and embedded abrasive particles. A dense array of copper or copper alloy features is typically formed in a dielectric layer, such as a silicon oxide layer, by a damascene technique wherein trenches are initially formed. A barrier layer, such as a tantalum-containing layer, *e.g.*, tantalum (Ta), or tantalum nitride (TaN), is then conformally deposited on the exposed surfaces of the trenches and on the upper surface of the dielectric layer. Copper or a copper alloy is then deposited, as by electroplating, electroless plating, physical vapor deposition (PVD) or chemical vapor deposition (CVD) on the barrier layer, typically at a thickness between about 8,000Å and about 18,000 Å.

CMP is then conducted to remove the copper or copper alloy overburden stopping on the barrier layer followed by barrier layer removal, employing a mixture of a chemical agent and abrasive particles, to remove the barrier layer, or conducting CMP directly down to the dielectric layer. Copper or copper alloy overburden is material deposited on the substrate in excess of the required amount to fill features formed on the substrate surface. Buffing is optionally conducted on the dielectric layer surface to remove defects, such as scratches in the dielectric materials and further planarize the dielectric material, leaving a copper or the copper alloy filling the damascene opening. The resulting copper or copper alloy filling the dual damascene has an exposed upper surface typically having a high concentration of surface defects. These defects include corrosion, *e.g.*, corrosion stains, microscratches, micropitting and surface abrasive particles. Copper and copper alloy wafers exhibit a much greater tendency to scratch during planarization than dielectric materials, such as oxides or nitrides. Copper and copper alloy surfaces corrode very easily and are difficult to passivate in low pH aqueous environments. Conventional wafer cleaning alone cannot completely eliminate such defects. Conventional practices for

planarizing copper or copper alloys disadvantageously result in a high defect count subsequent to planarization. Such surface defects adversely impact device performance and reliability, particularly as device geometries shrink into the deep sub-micron range. Therefore, there exists a need for methodology enabling the planarization of copper and copper alloys with a reduced amount of surface defects. There exists a further need for such enabling methodology that is compatible with conventional polishing techniques and apparatus.

SUMMARY OF THE INVENTION

Aspects of the invention generally provide a method and composition for planarizing a substrate surface including planarizing metals, such as copper and copper alloys, with reduced surface defects and surface corrosion.

In one aspect, the invention provides a method of treating a substrate surface comprising copper or a copper alloy, the method comprising applying to the substrate surface a composition comprising one or more chelating agents, a pH adjusting agent to produce a pH between about 3 and about 11, and deionized water, and then applying a corrosion inhibitor solution. The method may use a composition further including a corrosion inhibitor and/or a reducing agent. The method may further comprise treating the substrate surface with the corrosion inhibitor solution prior to treating the substrate surface with the composition.

In another aspect, the invention provides a method for planarizing a substrate surface containing a dielectric layer having an upper surface and at least one opening, a barrier layer lining the opening and on the upper surface of the dielectric layer, and copper or a copper alloy filling the opening and the dielectric layer, the method comprising removing the copper or copper alloy layer and the barrier leaving an exposed substrate surface comprising copper or copper alloy, and treating the exposed substrate surface comprising copper or the copper alloy by applying thereto a composition comprising one or more chelating agents, a pH adjusting agent to produce a pH between about 3 and about 11, and deionized water, and then applying a corrosion inhibitor solution. The composition may further include a corrosion inhibitor and/or a pH adjusting agent. The method may further comprise removal of the barrier layer removal after removing the

copper or copper alloy layer and prior to chemically treating the exposed substrate surface. The method may further comprise treating the substrate surface with the corrosion inhibitor solution prior to applying the composition.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1-4 illustrate processing step of a method in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Embodiments of the present invention described herein enable effective and efficient planarization of a substrate surface having copper or copper alloy containing features with significantly reduced defects, such as corrosion, scratches, pitting and embedded abrasive particles, consistent with the ever increasing demands for reliable interconnect patterns having feature sizes in the deep submicron range. As used throughout this disclosure, copper or copper alloy is intended to encompass high purity elemental copper as well as copper-based alloys, *e.g.*, copper-based alloys containing at least about 80 wt.% copper.

Embodiments of the invention described herein can be advantageously used in a strategic multi-step process subsequent to CMP and barrier layer removal. The multi-step methodology of embodiments of the invention treat the surface of the substrate generated during CMP copper or copper alloy layer and barrier layer removal leaving a substrate surface with reduced surface defects and passivated from oxidation and other processes that can cause the formation of defects in the substrate surface following CMP processing. The treatment of the substrate surface can comprise removing a thin surface layer of the processed substrate, such as copper or copper alloy containing features formed in the substrate surface, and/or removing corrosion stains, typically copper oxide and/or copper hydroxide mixed with corrosion by-products.

The multi-step methodology of embodiments of the invention comprise treating the exposed substrate surface of copper or copper alloy containing features after barrier layer removal including applying an optional corrosion inhibitor solution, a composition including one or more chelating agents, such as an acid, *e.g.*, citric acid, and/or a base, *e.g.*,

ammonium hydroxide and/or an amine, one or more pH adjusting agents to produce a pH between about 3 and about 11, and deionized water, and then applying a corrosion inhibitor solution. The composition may further include a corrosion inhibitor and/or a reducing agent.

The exact mechanism underpinning the reduction of defects and surface passivation achieved by embodiments of the invention is not known with certainty. However, it is believed that the treatment in accordance with embodiments of the invention subsequent to barrier layer removal removes a thin layer of the surface of the copper or copper alloy containing features containing defects and/or removes corrosion stains leaving a relatively defect free surface, and promptly passivates the relatively defect free surface to avoid the generation of further defects. It is believed that the optional initial treatment with a corrosion inhibitor and deionized water reduces corrosion, particularly corrosion induced by an abrasive slurry used on the surface of the copper or copper alloy containing features. Corrosion, unlike static etching, is non-uniform and, hence, should be avoided.

The optional initial treatment with a corrosion inhibitor solution can comprise the use of any of various corrosion inhibitors, such as benzotriazole (BTA) or 5-methyl-1-benzotriazole (TTA) present in an amount between about 0.01 wt.% and about 0.50 wt.% corrosion inhibitor and deinonized water. In one aspect, the corrosion inhibitor solution includes about 0.05 wt.% corrosion inhibitor and deionized water. The initial treatment comprises exposing the surface of the substrate for between about 3 seconds and about 10 seconds, *e.g.* In one aspect of the process, the corrosion inhibitor solution is applied for about 5 seconds.

The substrate surface is treated with a composition treating the exposed surface comprising copper or the copper alloy by applying thereto a composition including one or more chelating agents, a pH adjusting agent to produce a pH between about 3 and about 11, and deionized water, and then applying a corrosion inhibitor solution. The composition may further comprise a corrosion inhibitor and/or a reducing agent. In one aspect of the invention, the composition may be diluted between a saturated composition to a very dilute solution of about 1 vol% of the composition. In one aspect, the

composition is diluted with deionized water between about 5 vol% and about 10 vol% of the original composition.

It is believed that a subsequent treatment with the composition effects removal of up to about 50Å of the surface of the features disposed in the substrate surface and/or corrosion stains, generated by surface corrosion, microscratching and pitting, leaving a substantially defect free surface. This surface treatment can be conducted by application of the composition between about 10 seconds and about 20 seconds.

The one or more chelating agents may include an acid, a base, or a combination thereof. The acid may include an organic acid, such as a carboxylic acid having one or more acid groups. Examples of acids suitable for use in the composition include acetic acid, citric acid, maleic acid, and combinations thereof. The acid can be present in an amount up to about 40 wt.% of the composition. In one aspect of the composition, the acid comprises between about 5 wt.% and about 30 wt.% of the composition. The acid may also perform as a chelating agent in the composition, for example, acetic acid may perform as a chelating agent for copper or copper alloys. When a diluted solution of the composition is used for cleaning the substrate surface, the acid preferably has a concentration between about 2 wt.% and about 10 wt.% of the diluted composition.

The base may include ammonium hydroxide, ammonium hydroxide derivatives, amines, and combinations thereof. Examples of amines include primary amines, such as methylamine and ethylamine, secondary amines, and combinations thereof. The base may include compounds having one or more amine groups or amide groups, such as ethylenediaminetetraacetic acid, methylformamide, or ethylenediamine. An example of an ammonium hydroxide derivative is tetramethyl ammonia hydroxide. The base can be present in an amount up to about 5 wt.% of the composition. In one aspect, the base includes between about 0.5 wt.% and about 3.0 wt.% of the composition. The base may also perform as a chelating agent in the composition, for example, ammonium hydroxide may perform as a chelating agent for copper or copper alloys. Generally, acids and bases that may perform as chelating agents chemically react with material, such as metal ions, from the surface of the substrate or in the composition to form a soluble metal complex for removal from the surface of the substrate.

The one or more pH adjusting agents may include non-oxidizing organic and

inorganic acids or bases. The pH adjusting agent is generally in an amount sufficient to generate or maintain a desired pH between about 3 and about 11, such as an acidic pH, for example a pH of about 3, or a neutral pH, *e.g.*, a pH between about 6 and about 8. In one aspect, the composition has a pH between about 3 and about 7. Examples of pH adjusting agents include bases such as potassium hydroxide (KOH), and/or inorganic and/or organic acids, such as acetic acid, phosphoric acid, or oxalic acid.

An acidic pH adjusting agent may be used with a basic chelating agent; a basic pH adjusting agent may be used with an acidic chelating agent; and both acidic and basic pH adjusting agents may be used with a combination of acidic and basic chelating agents. The one or more pH adjusting agents may include acidic chelating agents, basic chelating agents, or a combination thereof in the composition.

Corrosion inhibitors, such as any various organic compounds containing an azole group, including benzotriazole (BTA), mercaptobenzotriazole, or 5-methyl-1-benzotriazole (TTA), can be added to the composition in a amount between about 0.01 wt.% and about 0.50 wt.% of the composition. In one aspect, the corrosion inhibitor comprises about 0.05 wt.% of the composition.

Additionally, a reducing agent may be added to the composition to enhance removal of surface defects. The reducing agent can be selected from the group of hydroxylamine, glucose, sulfothionate, potassium iodide, and combinations thereof. The reducing agent can be present in an amount between about 0.01 wt.% to about 20 wt.% of the composition. In one aspect, the reducing agent comprises between about 0.01 wt.% to about 5 wt.% of the composition. In one aspect of the invention, a concentration of about 0.1 wt.% of reducing agent is used in the composition.

The corrosion inhibitor solution is then applied to the substrate surface. It is believed that the final treatment with the corrosion inhibitor solution described herein, such as TTA in deionized water, protects the surface during de-chucking and provides a passivated surface layer protecting the substantially defect-free surface of the copper or copper alloy containing features and substrate surface from attack by dissolved oxygen.

Embodiments of the invention described herein include removing the copper or copper alloy overburden and barrier layer in any of various conventional manners. For example, the copper or copper alloy overburden and barrier layer can be removed during a

single stage CMP technique, or the copper or copper alloy overburden can be initially removed by CMP followed by removing the barrier layer. In either case, the substrate surface including the exposed surface of the copper or copper alloy containing features can be subjected to an additional buffing step to remove defects prior to performing the multi-step procedure of embodiments of the invention. Buffing is broadly defined herein as a contacting a substrate with a polishing pad and a chemical composition or de-ionized water with low or minimal pressure between the polishing pad and the substrate to remove surface defects and particulate matter from the substrate surface. Buffing is typically performed with a soft polishing in the absence of abrasive materials. CMP of the copper or copper alloy layer and barrier layer removal can be implemented in a conventional manner.

Conventional substrates and dielectric layers are encompassed by embodiments of the invention. For example, the substrate can be doped monocrystalline silicon or gallium-arsenide. The dielectric layer can comprise any of various dielectric materials conventionally employed in the manufacture of semiconductor devices. For example, dielectric materials, such as silicon dioxide, phosphorus-doped silicon glass (PSG), boron- and phosphorous-doped silicon glass (BPSG) and silicon dioxide derived from tetraethyl orthosilicate (TEOS) or silane by plasma enhanced chemical vapor deposition (PECVD) can be employed. Dielectric layers in accordance with embodiments of the invention can also comprise low dielectric constant materials, including polymers, such as polyimides, and carbon-containing silicon dioxide, *e.g.*, Black Diamond™ dielectric material available from Applied Materials, Inc., located in Santa Clara, California. The openings are formed in dielectric layers by conventional photolithographic and etching techniques.

An embodiment of the invention is schematically illustrated in Figures 1-4, wherein similar features bear similar reference numerals. Referring to Figure 1, dielectric layer 10, *e.g.*, silicon oxide, is formed overlying a substrate (not shown). A plurality of openings 11 are formed in a designated area A in which a dense array of conductive lines are to be formed bordering an open field B. A barrier layer 12, *e.g.*, TaN, is deposited lining the openings 11 and on the upper surface of silicon oxide dielectric layer 10. Typically, the openings 11 are spaced apart by a distance C which is less than about 1

micron, *e.g.*, about 0.2 micron. Copper layer 13 is then deposited at a thickness D between about 8,000Å and about 18,000Å.

Referring to Figures 1 and 2, CMP is initially conducted in a conventional manner to remove the copper overburden stopping on TaN barrier layer 12. As shown in Figures 2 and 3, barrier layer removal is conducted in a conventional manner to remove TaN layer 12. The resulting copper interconnection structure comprises a dense array A of copper lines 13 bordered by open field B. However, the upper surface 40 of the copper containing feature and the dielectric surface 41 exhibit an unacceptably high defect count, *e.g.*, measured at best of at least 750 defects, comprising primarily corrosion stains, microscratches, micropits and abrasive slurry particles.

In accordance with one embodiment of the invention described herein, the copper containing feature surface 40 and dielectric surface 41 are treated by a multi-step procedure comprising applying an optimal solution of a corrosion inhibitor, followed by a composition comprising one or more chelating agents, a pH adjusting agent to produce a pH between about 3 and about 11, and deionized water, and then applying a solution of a corrosion inhibitor. The optional initial treatment with a corrosion inhibitor solution can comprise deionized water and between about 0.01 and about 0.50 wt.%, *e.g.*, about 0.05 wt.%, of a corrosion inhibitor, such as BTA or TTA. In one aspect, the corrosion inhibitor solution comprises about 0.05 wt.% corrosion inhibitor and deionized water. The optional initial treatment is performed for a period between about 3 and about 10 seconds, *e.g.*, about 5 seconds.

The composition is then applied to the substrate to treat the substrate surface. The composition, for example, may comprise up to about 40 wt.% of an acid, *e.g.*, between about 5 and about 30 wt.% citric acid, up to about 5 wt.% of ammonium hydroxide, ammonium hydroxide derivatives, amines, and combinations thereof, *e.g.*, between about 0.5 and about 3.0 wt.% ammonium hydroxide, the remainder deionized water. The composition has a pH between about 4 and about 5.

One embodiment of the composition described herein that has been observed to produce effective results includes about 26 wt.% citric acid, about 3 wt.% ammonia, deionized water, and has a pH of about 4.

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The composition is applied to the substrate surface for a suitable period of time, *e.g.*, between about 10 seconds and about 30 seconds.

Subsequently, the substrate is de-chucked while applying thereto a corrosion inhibitor, such as TTA or BTA in deionized water. The treatment with an optional corrosion inhibitor, followed by cleaning with the composition described herein, and de-chucking with a corrosion inhibitor, effectively removes a defective upper surface of the copper or copper alloy containing feature 40 and dielectric surface 41 leaving a relatively defect-free passivated surface 50, as shown in Figure 4. Experiments conducted employing the inventive procedure resulted in a planarized substrate surface having copper or copper alloy containing features having a surface with a defect count less than 139, even less than 100, as measured.

Embodiments of the invention described herein are applicable to planarizing a substrate surface during various stages of semiconductor manufacturing employing any of various types of CMP systems. Embodiments of the invention described herein enjoy particular applicability in the manufacture of high density semiconductor devices with metal features in the deep submicron range.

While foregoing is directed to the preferred embodiment of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.